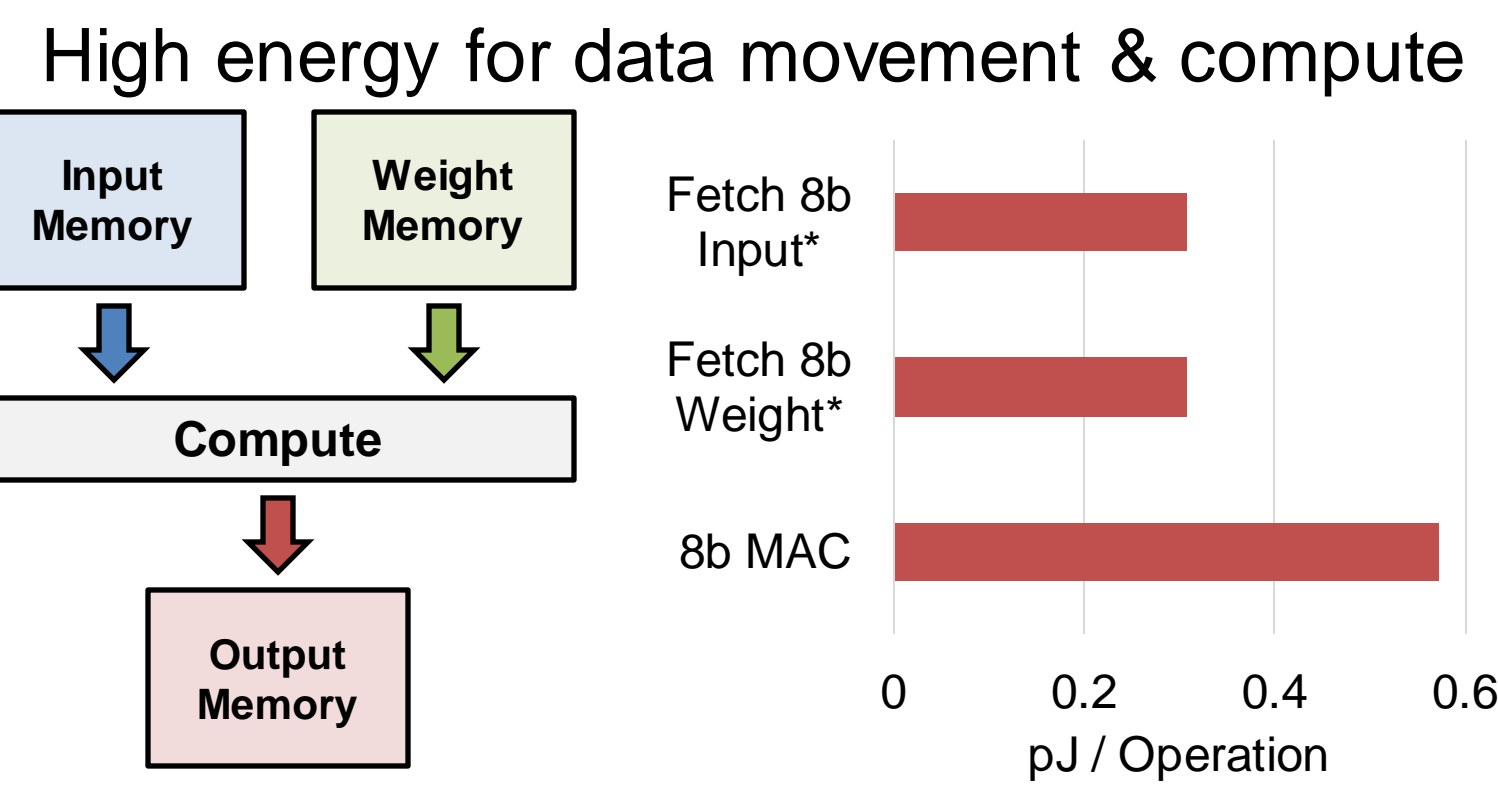


# RAELLA: Reforming the Arithmetic for Efficient, Low-Resolution, and Low-Loss Analog PIM: No Retraining Required!

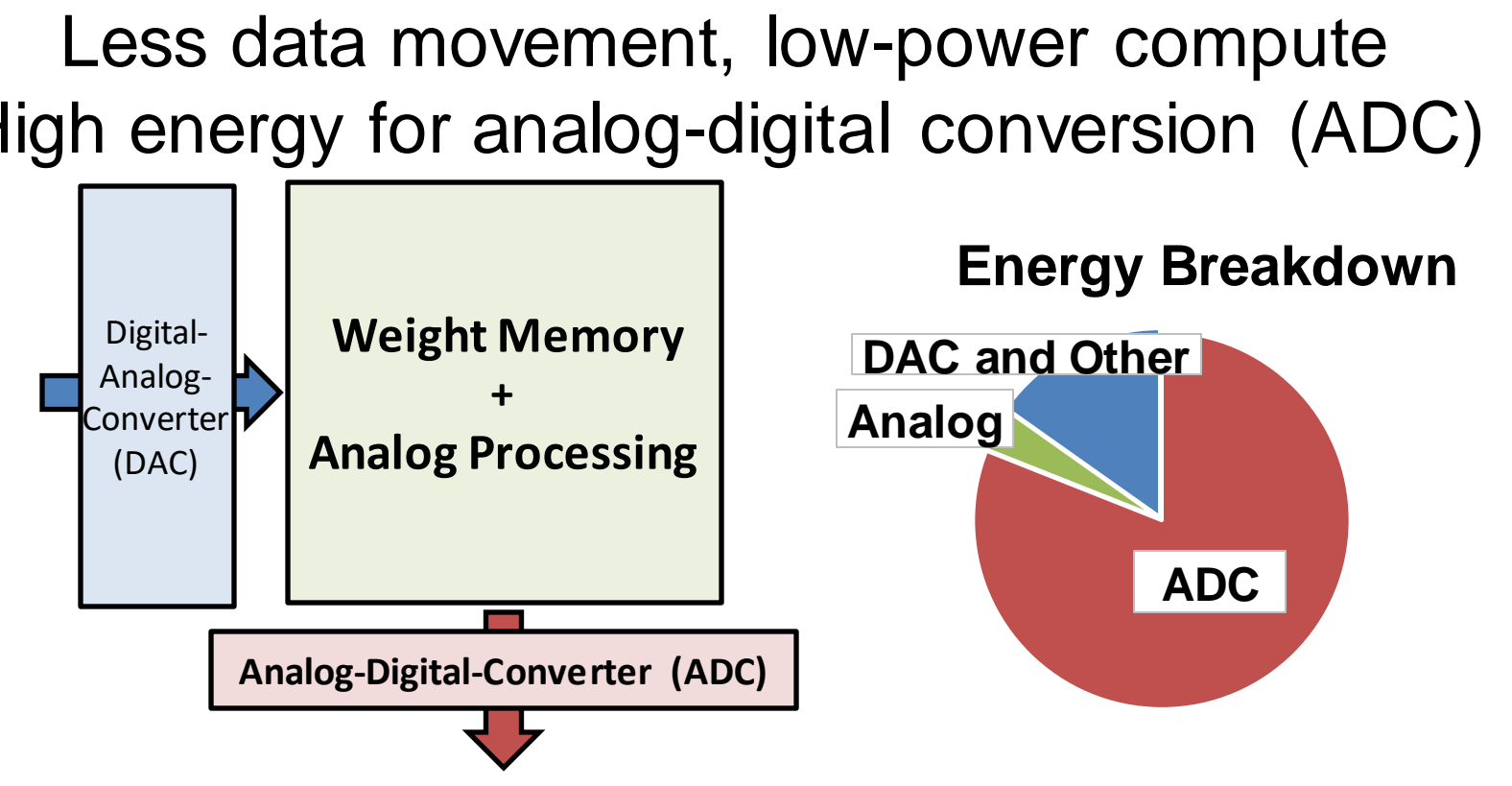
Tanner Andrusis, Joel S. Emer, Vivienne Sze

## Motivation

### Conventional Deep Neural Network (DNN) Accelerator

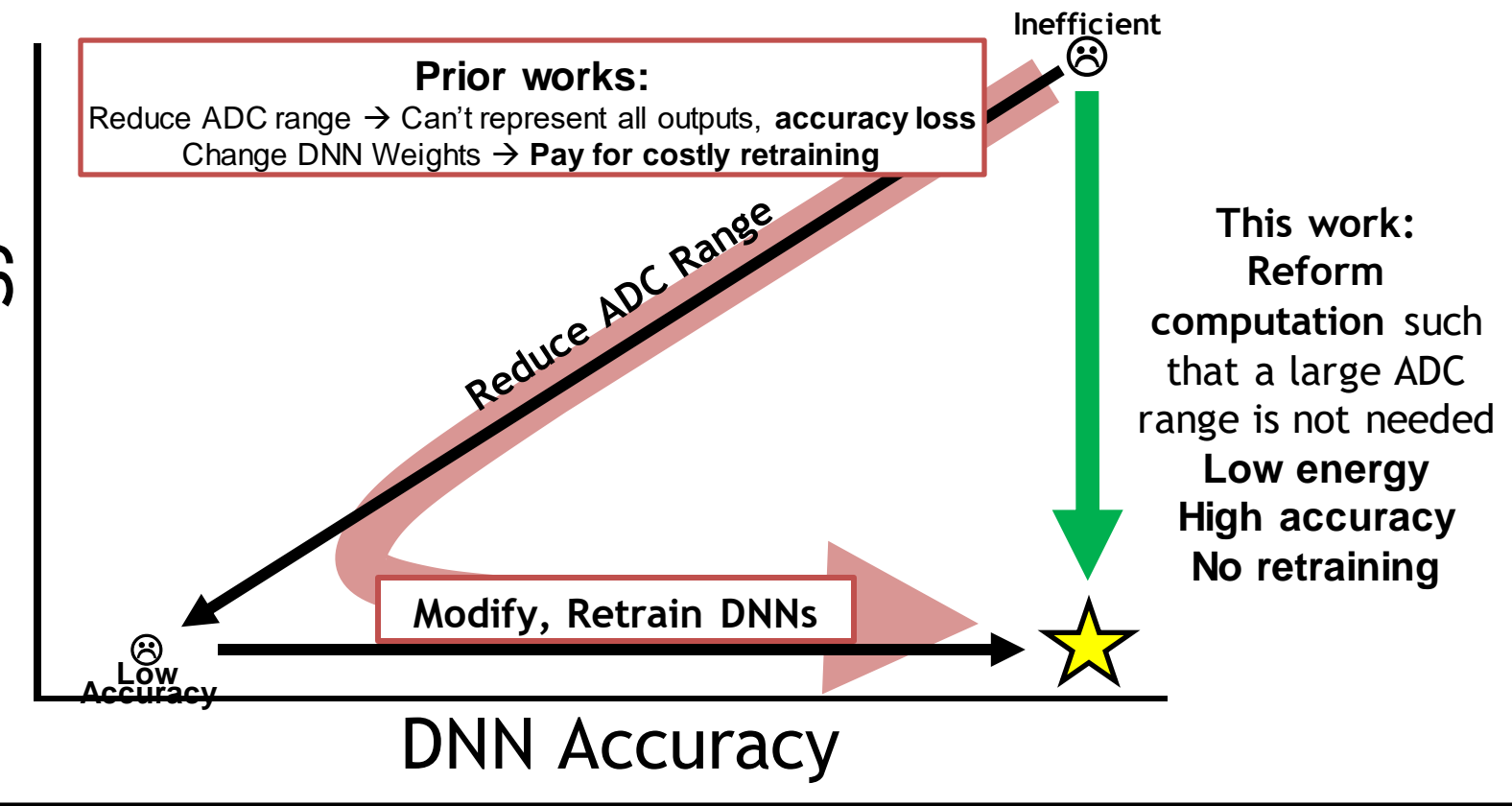


### Processing in Memory (PIM) DNN Accelerator

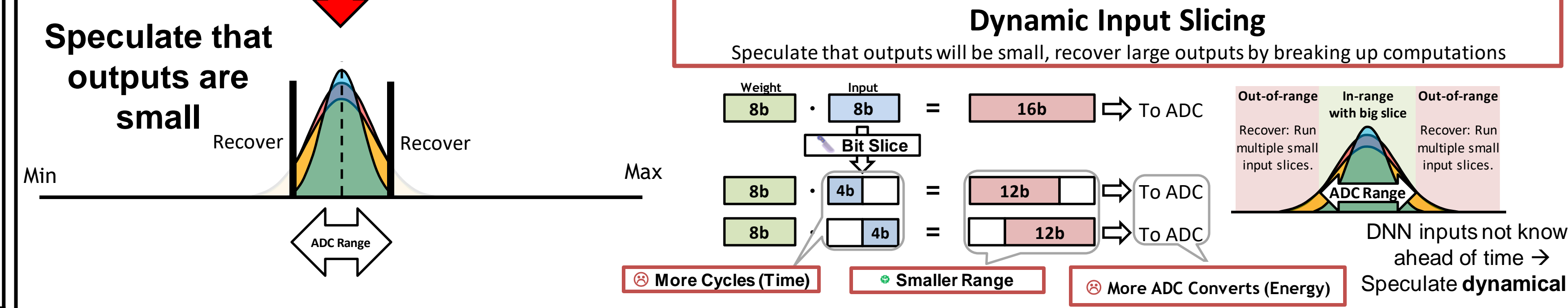
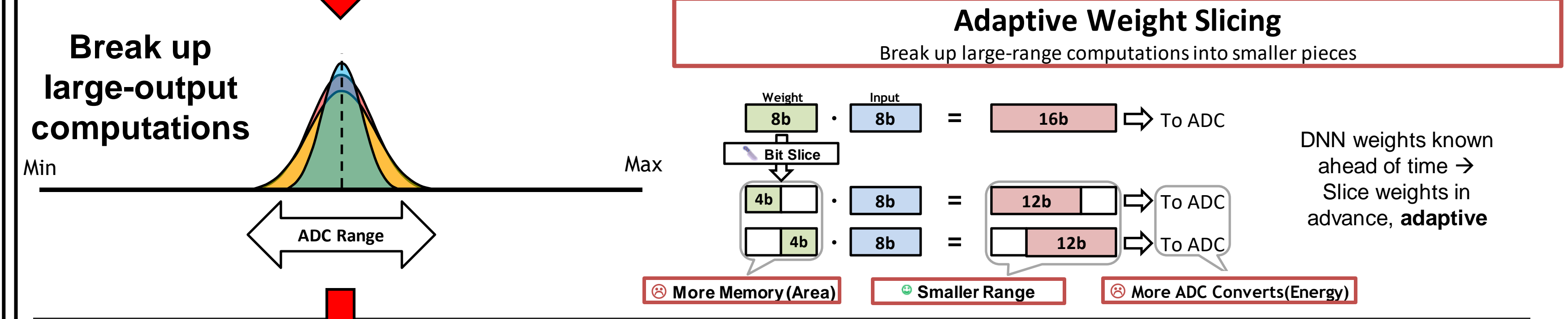
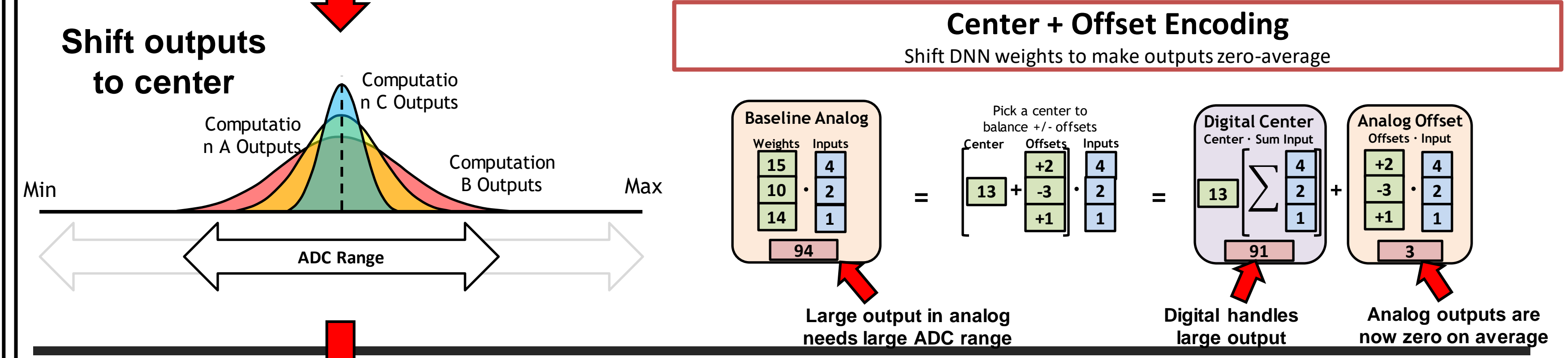
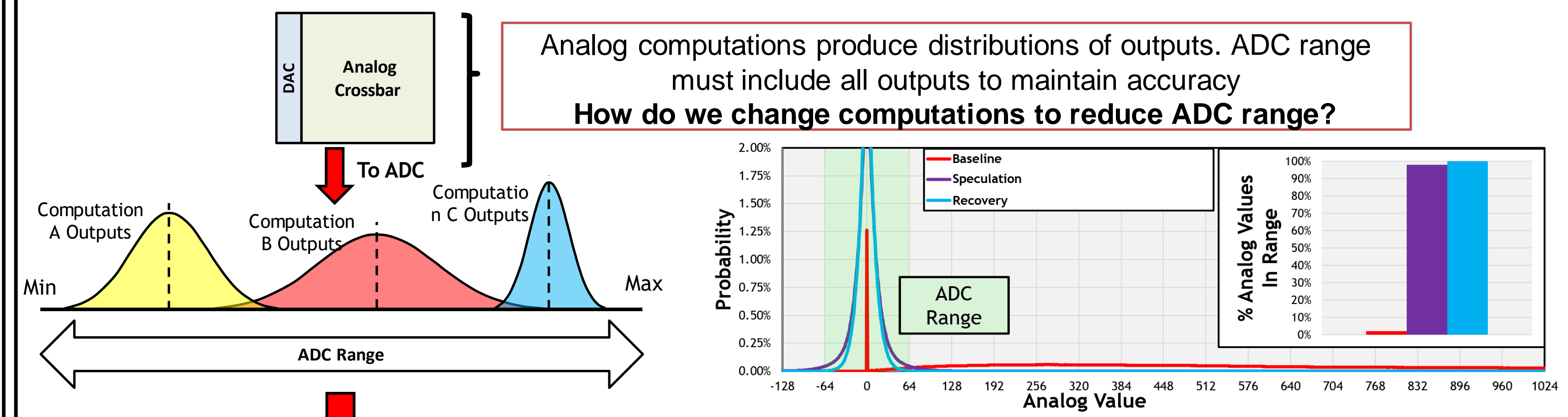


### ADC Energy Increases with ADC Range

Reduce ADC range → Save energy



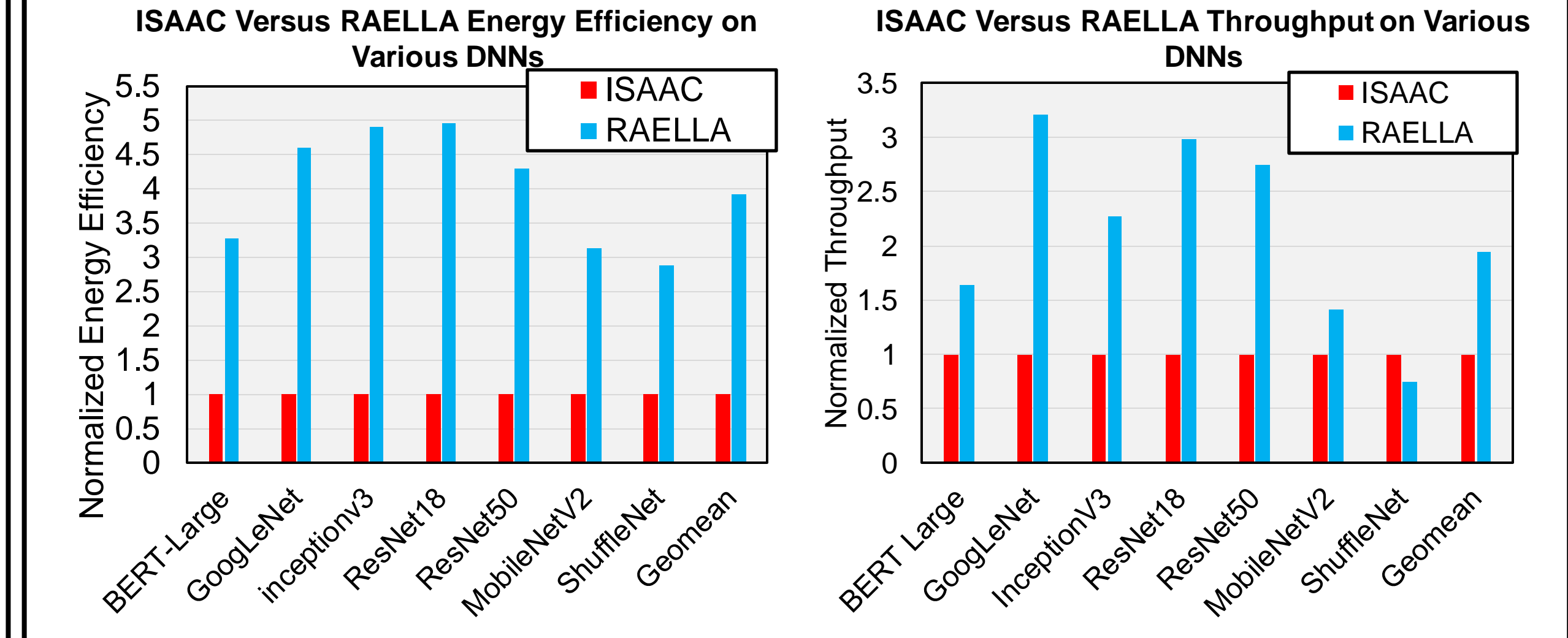
## Methods: Change Arithmetic to Reduce ADC Range



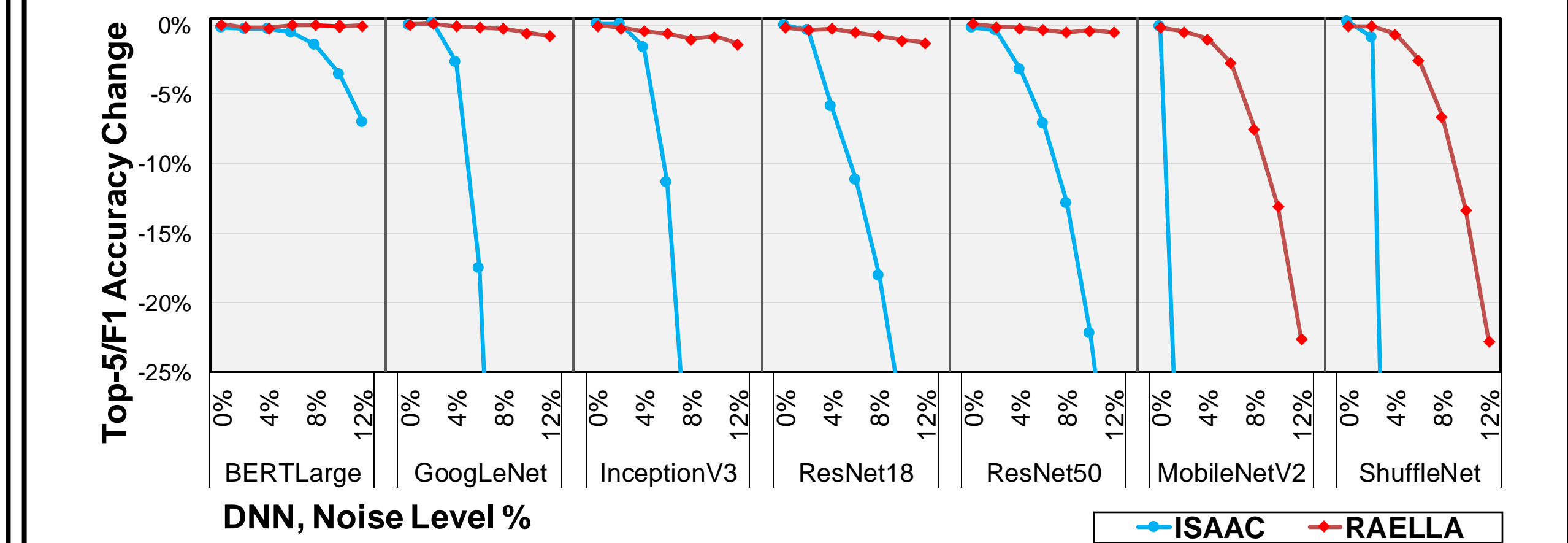
## Results: Impacts of a lower-range ADC

Compare to popular PIM DNN accelerator ISAAC

Less ADC energy → Up to 5x higher energy efficiency,  
Less ADC area, spend more chip area on compute → 3x higher throughput



Partition analog/digital compute + adaptive & dynamic strategies → **Protect from noise-induced accuracy loss**



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Artifact: <https://github.com/mit-emze/raella>